Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A bumping process, comprising:
providing a wafer having a plurality of bonding pads and a passivation layer having a plurality openings thereon, wherein the bonding pads are exposed out of the openings of the passivation layer;
forming an under-bump-metallurgy layer on the wafer and covering the bonding pads;
forming a first photoresist layer over the wafer to cover the bonding pads and the passivation layer;
forming a second photoresist layer on the first photoresist layer, wherein the first photoresist layer has exposure/development characteristics different from that of the second photoresist layer;
performing a single exposure process to the first and second photoresist layers to form a plurality of first openings in the first photoresist layer and a plurality of second openings in the second photoresist layer simultaneously, wherein a plurality of stair-shaped openings are formed from the first openings and the second openings and expose the under-bump-metallurgy layer;
filling a solder material into the stair-shaped openings to form a plurality of solder posts; and

removing the first photoresist layer and the second photoresist layer.

[c2] 2. The bumping process of claim 1, further comprising reflowing the solder posts to form a plurality of bumps over the under-bump-metallurgy layer, after removing the first and second photoresist layers.

[c3] 3. The bumping process of claim 1, wherein the first openings are smaller than the second openings.

[c4] 4. The bumping process of claim 1, wherein the first photoresist layer has a photosensitivity lower than that of the second photoresist layer.

[c5] 5. The bumping process of claim 1, wherein the first photoresist layer comprises a spin-coated photoresist or a dry film.

[c6] 6. The bumping process of claim 1, wherein the second photoresist layer is a liquid state spin-coated photoresist or a dry film.

[c7] 7. The bumping process of claim 1, wherein the method of filling the solder material comprises electroplating or stencil printing.

[c8] 8. A bumping process, comprising:
providing a wafer having a plurality of bonding pads and

a passivation layer having a plurality of openings thereon, wherein the bonding pads are exposed out of the openings of the passivation layer;

forming an under-bump-metallurgy layer on the wafer to cover the bonding pads;

forming a plurality of photoresist layers on the wafer to cover the bonding pads and the passivation layers, wherein the photoresist layers have different photosensitivities;

forming a plurality of stair-like openings located above the bonding pads in the photoresist layers by an exposure process, wherein the under-bump-metallurgy layer is exposed out of the stair-shaped openings;

filling a solder material into the stair-shaped openings to form a plurality solder posts; and

removing the photoresist layers.

[c9] 9. The bumping process of claim 8, further comprising the step of reflowing the solder posts to form a plurality of bumps on the metal layer, after removing the photoresist layers.

[c10] 10. The bumping process of claim 8, wherein a size of the stair-like openings in the lower photoresist layer that is closer to the bonding pads is smaller than that of the stair-shaped openings in the higher photoresist layer that is farther away from the bonding pads.

[c11] 11. The bumping process of claim 8, wherein the photoresist layer that is farthest away from the bonding pads has the highest photosensitivity, while the photoresist layer that is closest to the bonding pads has the lowest photosensitivity.

[c12] 12. The bumping process of claim 8, wherein the photoresist layers comprise a spin-coated photoresist.

[c13] 13. The bumping process of claim 8, wherein the photoresist layers comprise a dry film.

[c14] 14. The bumping process of claim 8, wherein the method of filling the solder material comprises electroplating or stencil printing.